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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/730,834	12/08/2003	Nick Kuo	JCLA11759	5204

27765 7590 01/24/2007

NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION
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MERRIFIELD, VA 22116

EXAMINER	
ANDUJAR, LEONARDO	
ART UNIT	PAPER NUMBER
2826	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/24/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/730,834	KUO ET AL.	
	Examiner	Art Unit	
	Leonardo Andújar	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED. (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 November 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3,5,13,15-21,23-35,37-44 and 46-52* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *27-35,37-44 and 46-52* is/are allowed.

6)☒ Claim(s) *1,3,5,13,15-21, 25 and 26* is/are rejected.

7)☒ Claim(s) *23 and 24* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Acknowledgment

1. The amendment filed on 11/06/2006 in response to the Office action mailed on 07/05/2006 has been entered. The present Office action is made with all the suggested amendments being fully considered. Accordingly, pending in this Office action are claims 1, 3, 5-1, 13, 15-21, 23-35, 37-44 and 46-52.

Election/Restrictions

2. Applicant's election without traverse of species 4 (figs. 1d and 2d) in the reply filed on 9/07/2005 is acknowledged

Claim Rejections - 35 USC § 103

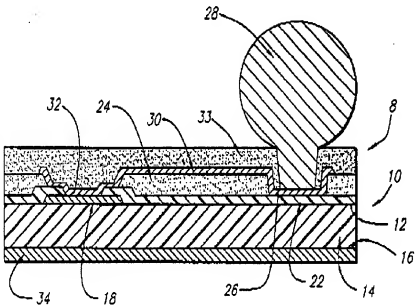
3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 3, 8-11, 13, 17, 19, 20, 25 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Elenius et al. (US 6,287,893) in view of Kim (US 5,854,513) further in view of Sato et al. (US 4,051,508).

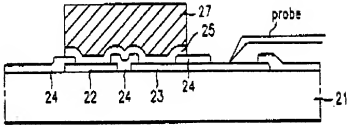
5. Regarding claims 1 and 3, Elenius (e.g. figs. 1 & 2) shows a substrate 14, a metallization structure 18 over the semiconductor substrate; a passivation layer 22 over the metallization structure 18, wherein an opening in the passivation layer exposes a top surface of the metallization structure and a patterned circuit 30 connected to the top

surface though the opening, wherein the patterned circuit layer comprises a first portion having a bump 28 formed thereover and a second portion connected to the first portion (col. 1/lls. 22-45 & col. 6/lls. 1-37).



Elenius does not teach a testing pad or second portion used to be in contact with a testing probe and/or a patterned circuit layer comprising a gold layer. Therefore, Elenius in view of Kim does not teach that the gold layer has a thickness greater than one micron. Nevertheless, Kim (e.g. fig. 3) shows a patterned circuit layer connected to a top surface though an opening wherein the patterned circuit layer comprises a first portion used to have a bump 27 formed thereover and a second portion to be in contact with a testing probe whereon the firs portion is connected to the second portion. This type of embodiment prevent decreases in testing reliability caused by damages on the surface of the bump and polluting material thereby enhancing its yield with respect to bonding (col. 2/lls. 10-30).

FIG.3



On the other hand, Sato teaches that pattern circuit layer comprising a gold layer of 2 microns (col. 34/35). It would have been obvious to one of ordinary skill in the art at the time the invention was made to include a second portion used to be in contact with a probe to prevent decreases in testing reliability caused by damages on the surface of the bump and polluting material during the testing process, thereby enhancing its yield with respect to bonding as taught by Kim and to make the pattern circuit layer disclosed by Elenius in view of Kim comprising gold layer of 2 microns as suggested by Sato to increase the electrical conductivity of the patterned circuit layer and because it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. In re Leshin, 125 USPQ 416

6. Regarding claims 8 and 9, Elenius teaches a polymer layer 24 (e.g. polyimide) between the passivation layer and the patterned circuit layer (col. 6/lls. 51-56).

7. Regarding claims 10 and 11, Elenius in view of Kim further in view of Sato shows a polymer layer 33 (e.g. polyimide) on the patterned circuit layer, multiple openings in the polymer layer exposing the first portion and the second portions (see Elenius, col.

7/lls. 50-54). Note that Kim shows a first opening exposing the first portion and a second opening exposing the second portions.

8. Regarding claim 13, Elenius in view of Kim further in view of Sato shows that the patterned circuit comprises a metal line connecting the first and second portions.

9. Regarding claim 17, Elenius shows a bump on the first portion.

10. Regarding claim 19, Elenius discloses that the bump comprises a solder (col. 7/ll. 62).

11. Regarding claims 25 and 26, Elenius in view of Kim further in view of Sato teaches most aspects of the instant invention except for the specific pitch between first and second portion is less than 300 micrometers or less than 1 micrometer. However, it is known in the art that pitches are subjected to optimization, it is desirable to minimize the pitch between two contact areas the downscaling of the minimum feature sizes of the device. It would have been obvious to one of ordinary skill in the art at the time the invention was made to minimize the pitch between the first and second portions disclosed by Elenius in view of Kim to effectively reduce the overall device's size as it is known in the art. With regards to the specific pitches claimed by applicant i.e., a less than 300 micrometers or less than 1 millimeter, absent of any criticality is only considered to be the "optimum" pitch of the pitch disclosed by the Prior Art that a person having ordinary skill in the art would have been able to determine using routine experimentation based, among other things, on the desired accuracy, size reduction, manufacturing costs, etc. (see In re Boesch, 205 USPQ 215 (CCPA 1980)), and since neither non-obvious nor unexpected results, i.e., results which are different in kind and

not in degree from the results of the prior art, will be obtained as long as filled groove is used as already suggested by the Prior Art. Moreover, the specification contains no disclosure of either the critical nature of the claimed arrangement or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the applicant must show that the chosen dimensions are critical. In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

12. Claims 1, 5, 6, 7, 17, 18 and 20, are rejected under 35 U.S.C. 103(a) as being unpatentable over Elenius et al. (US 6,287,893) in view of Kim (US 5,854,513) further in view of Lee (US 20040036170).

13. Regarding claims 1 and 5-7, Elenius (e.g. figs. 1 & 2) shows a substrate 14, a metallization structure 18 over the semiconductor substrate; a passivation layer 22 over the metallization structure 18, wherein an opening in the passivation layer exposes a top surface of the metallization structure and a patterned circuit 30 (e.g. UBM) connected to the top surface though the opening, wherein the patterned circuit layer comprises a first portion having a bump 28 formed thereover and a second portion connected to the first portion (col. 1/lls. 22-45; col. 6/lls. 1-37 & col. 7/lls. 7-35). Elenius does not teach a testing pad or second portion used to be in contact with a testing probe and/or a patterned circuit layer comprising a gold layer. Therefore, Elenius in view of Kim does not teach that a nickel layer under the gold layer or a copper layer under the gold layer. Nevertheless, Kim (e.g. fig. 3) shows a patterned circuit layer connected to a top surface though an opening wherein the patterned circuit layer comprises a first

portion used to have a bump 27 formed thereover and a second portion to be in contact with a testing probe whereon the firs portion is connected to the second portion. This type of embodiment prevent decreases in testing reliability caused by damages on the surface of the bump and polluting material thereby enhancing its yield with respect to bonding (col. 2/lls. 10-30). Lee teaches an UBM comprising a copper layer, a gold layer over the copper layer and a nickel layer therebetween (pp 0006). It would have been obvious to one of ordinary skill in the art at the time the invention was made to include a second portion used to be in contact with a probe to prevent decreases in testing reliability caused by damages on the surface of the bump and polluting material during the testing process, thereby enhancing its yield with respect to bonding as taught by Kim and to make the pattern circuit layer/UBM disclosed by Elenius in view of Kim comprising copper layer, a gold layer over the copper layer and a nickel layer therebetween as suggested by Lee to increase the electrical conductivity of the patterned circuit layer and because it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. In re Leshin, 125 USPQ 416.

14. Regarding claim 17, Elenius shows a bump on the first portion.

15. Regarding claim 18, Elenius in view of Kim further in view of Lee discloses a nickel layer between the bump and the first portion.

16. Regarding claim 20, Elenius in view of Kim further in view of Lee discloses a copper layer between the bump and the first portion.

17. Claims 15 and 16, are rejected under 35 U.S.C. 103(a) as being unpatentable over Elenius et al. (US 6,287,893) in view of Kim (US 5,854,513) further in view of Sato et al. (US 4,051,508) further in view of Kitayama et al. (US 5,646,439).

18. Regarding claims 15 and 16, Elenius in view of Kim further in view of Sato teaches most aspects of the instant invention including a passivation comprising a topmost layer of the electronic component. Elenius in view of Kim further in view of Sato does not disclose that the passivation layer comprise a nitride layer or a layer having a thickness greater than 0.35 micrometers. Nevertheless, Kitayama disclose that a passivation layer made of silicon nitride and having a thickness of more than 0.35 micrometer protects the wafer from moisture (col. 3/lls. 22-35). It would have been obvious to one having ordinary skill in the art at the time the invention was made to make the passivation layer disclosed by Elenius in view of Kim further in view of Sato of silicon nitride and having a thickness greater than 0.35 as suggested by Kitayama in order to protect the internal circuits formed within the wafer from moisture and because it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. In re Leshin, 125 USPQ 416.

19. Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Elenius et al. (US 6,287,893) in view of Kim (US 5,854,513) further in view of Sato et al. (US 4,051,508) further in view of Harper.

20. Regarding claim 21, Elenius in view of Kim further in view of Sato teaches most aspects of the instant invention including a bump. Elenius in view of Kim further in view

of Sato does not teach that the bump can be made of a lead free alloy. Nevertheless, Harper (e.g. table 5.3) teaches several suitable lead free solder alloys that are compatible with the surface mount technology. Harper's table 5.3 discloses melting ranges of common solder alloys. It would have been obvious to one of ordinary skill in the art at the time the invention was made to make the bump disclosed by Elenius in view of Kim further in view of Sato of a lead free alloy such as 95Sn/5Ag as suggested by Harper because this alloy has a relative high melting point, a high creep resistance (see table 5.5), it is more environmental friendly than lead alloys, and because it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. In re Leshin, 125 USPQ 416.

21. Claims 27-35, 37-44 and 46-52 are allowed.

22. Claims 23 and 24 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

23. Applicant's arguments have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

24. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

25. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

26. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leonardo Andújar whose telephone number is 571-272-1912. The examiner can normally be reached on Mon through Thu from 9:00 AM to 7:30 PM EST.

27. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sue Purvis can be reached on 571-272-1236. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

28. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Leonardo Andújar
Primary Examiner
Art Unit 2826

01/17/2007

Amendments to the Claims:

This listing of the Claims will replace all prior versions and listings of the claims in this patent application.

Listing of Claims:

1. (currently amended) A ~~circuitry~~ circuit component comprising:
   a semiconductor substrate;
   a metallization structure over said semiconductor substrate;
   a passivation layer over said metallization structure, wherein an opening in said passivation layer exposes a top surface of said metallization structure; and
   a patterned circuit layer connected to said top surface through said opening, wherein said patterned circuit layer comprises a first portion used to have a bump formed thereover and a second portion comprising a gold layer, wherein said gold layer is used to be in contact with a testing probe, and wherein said first portion is connected to said second portion. ~~used to be tested thereto.~~

2. (canceled)

3. (currently amended) The ~~circuitry~~ circuit component of Claim 1, wherein ~~said patterned circuit layer comprises a~~ said gold layer has ~~having~~ a thickness of greater than 1 micron.

4. (canceled)

5. (currently amended) The ~~circuitry~~ circuit component of Claim 1, wherein said patterned circuit layer comprises a nickel layer under said gold layer.

6. (currently amended) The ~~circuitry~~ circuit component of Claim 1, wherein said patterned circuit layer comprises a copper layer under said gold layer. ~~and a gold layer, said gold layer being over said copper layer.~~

7. (currently amended) The ~~circuitry~~ circuit component of Claim 1[[6]], wherein said patterned circuit layer further comprises a copper layer and a nickel layer over said copper layer, and wherein said gold layer is over said nickel layer. ~~between said copper layer and said gold layer.~~

8. (currently amended) The ~~circuitry~~ circuit component of Claim 1 further comprising a polymer layer between ~~over~~ said passivation layer~~, wherein~~ and said patterned circuit layer ~~is over said polymer layer~~.

9. (currently amended) The ~~circuitry~~ circuit component of Claim 8, wherein said polymer layer comprises polyimide.

10. (currently amended) The ~~circuitry~~ circuit component of Claim 1 further comprising a polymer layer on said patterned circuit layer, multiple openings ~~an opening~~ in said polymer layer exposing said first and second portions. ~~portion.~~

11. (currently amended) The ~~circuitry~~ circuit component of Claim 10, wherein said polymer layer comprises polyimide.

Claim 12 (canceled)

13. (currently amended) The ~~circuitry~~ circuit component of Claim 1, wherein said patterned circuit layer comprising a metal line ~~trace~~ connecting said first and second

portions.

Claim 14 (canceled)

15. (currently amended) The ~~circuitry~~ circuit component of Claim 1, wherein said passivation layer comprises a topmost nitride layer of said circuit ~~electronic~~ component.

16. (currently amended) The ~~circuitry~~ circuit component of Claim 1, wherein said passivation layer has a thickness of greater than 0.35 μm.

17. (currently amended) The ~~circuitry~~ circuit component of Claim 1 further comprising a bump on said first portion.

18. (currently amended) The ~~circuitry~~ circuit component of Claim 17 further comprising a nickel layer between said bump and said first portion.

19. (currently amended) The ~~circuitry~~ circuit component of Claim 17, wherein said bump comprises solder.

20. (currently amended) The ~~circuitry~~ circuit component of Claim 17 further comprising a copper layer between said bump and said first portion.

21. (currently amended) The ~~circuitry~~ circuit component of Claim 17, wherein said bump comprises a lead-free alloy.

Claim 22 (canceled)

23. (withdrawn and currently amended) The ~~circuitry~~ circuit component of Claim 1,

wherein said patterned circuit layer comprises a third portion used to be wirebonded thereto.

24. (withdrawn and currently amended) The ~~circuitry~~ circuit component of Claim 23, wherein said patterned circuit layer comprises a metal trace connecting said second and third portions.

25. (currently amended) The ~~circuitry~~ circuit component of Claim 1, wherein a ~~the~~ pitch between said first and second portions is less than 300 μm.

26. (currently amended) The ~~circuitry~~ circuit component of Claim 1, wherein a ~~the~~ pitch between said first and second portions is less than 1 millimeter.

27. (currently amended) A ~~circuitry~~ circuit component comprising:

a semiconductor substrate;

a metallization structure over said semiconductor substrate;

a passivation layer over said metallization structure, wherein an opening in said passivation layer exposes a top surface of said metallization structure; and

a patterned circuit layer connected to said top surface through said opening, wherein said patterned circuit layer comprises ~~a first metal layer and a second metal layer over said first metal layer, wherein said second metal layer has~~ a first portion used to have a bump formed thereover and a second portion comprising a copper layer, wherein said copper layer is used to be wirebonded thereover. ~~thereto.~~

28. (currently amended) The ~~circuitry~~ circuit component of Claim 27, wherein said patterned circuit layer further comprises a titanium-containing layer under said copper layer. ~~second metal layer comprises gold.~~

29. (currently amended) The ~~circuitry~~ circuit component of Claim 27, wherein said patterned circuit layer further comprises a chromium-containing layer under said copper layer. ~~second metal layer comprises copper.~~

30. (currently amended) The ~~circuitry~~ circuit component of Claim 27 further comprising a polymer layer between ~~over~~ said passivation layer~~, wherein~~ and said patterned circuit layer ~~is over said polymer layer~~.

31. (currently amended) The ~~circuitry~~ circuit component of Claim 30, wherein said polymer layer comprises polyimide.

32. (currently amended) The ~~circuitry~~ circuit component of Claim 27 comprising a polymer layer on said patterned circuit layer, multiple openings ~~an opening~~ in said polymer layer exposing said first and second portions. ~~portion.~~

33. (currently amended) The ~~circuitry~~ circuit component of Claim 32, wherein said polymer layer comprises polyimide.

34. (currently amended) The ~~circuitry~~ circuit component of Claim 27, wherein said patterned circuit layer comprises a metal line ~~trace~~ connecting said first and second portions.

35. (withdrawn and currently amended) The ~~circuitry~~ circuit component of Claim 27, wherein said patterned circuit layer comprises a third portion used to be in contact with a testing probe. ~~tested thereto.~~

Claim 36 (canceled)

37. (withdrawn and currently amended) The ~~circuitry~~ circuit component of Claim 35, wherein said patterned circuit layer comprises a metal trace connecting said first and third portions. ~~the pitch between said first and second portions is less than 300 μm.~~

38. (currently amended) The ~~circuitry~~ circuit component of Claim 27, wherein said passivation layer has a thickness of greater than 0.35 μm.

39. (currently amended) The ~~circuitry~~ circuit component of Claim 27, wherein said passivation layer comprises a topmost nitride layer of said circuit ~~electronic~~ component.

40. (currently amended) The ~~circuitry~~ circuit component of Claim 27 further comprising a bump over said first portion.

41. (currently amended) The ~~circuitry~~ circuit component of Claim 40, wherein said bump comprises solder.

42. (currently amended) The ~~circuitry~~ circuit component of Claim 40 further comprising a nickel ~~copper~~ layer between said bump and said first portion.

43. (currently amended) The ~~circuitry~~ circuit component of Claim 40, wherein said bump comprises a lead-free alloy.

44. (currently amended) The ~~circuitry~~ circuit component of Claim 27 further comprising a wirebonded wire bonded over said second portion.

Claim 45 (canceled)

46. (withdrawn and currently amended) A ~~circuitry~~ circuit component comprising:

a semiconductor substrate;

a metallization structure over said semiconductor substrate;

a passivation layer over said ~~over said~~ metallization structure, wherein an opening in said passivation layer exposes a top surface of said metallization structure; and

a patterned circuit layer connected to said top surface through said opening, wherein said patterned circuit layer comprises a first portion used to be wirebonded thereto and a second portion used to be in contact with a testing probe. ~~tested thereto.~~

47. (withdrawn and currently amended) The ~~circuitry~~ circuit component of Claim 46, wherein said patterned circuit layer comprises gold.

48. (withdrawn and currently amended) The ~~circuitry~~ circuit component of Claim 46, wherein said patterned circuit layer comprises a gold layer having a thickness of greater than 1 micron.

49. (withdrawn and currently amended) The ~~circuitry~~ circuit component of Claim 46, wherein said patterned circuit layer comprises copper.

50. (withdrawn and currently amended) The ~~circuitry~~ circuit component of Claim 46, wherein said patterned circuit layer comprises nickel.

51. (new) The circuit component of Claim 27, wherein said second portion further comprises a nickel layer over said copper layer, and wherein said nickel layer is used to be said wirebonded thereover.

52. (new) The circuit component of Claim 27, wherein said second portion further

comprises a gold layer over said copper layer, and wherein said gold layer is used to be said wirebonded thereon.

5

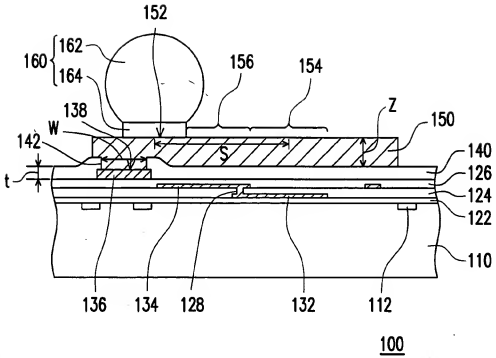


FIG. 1A

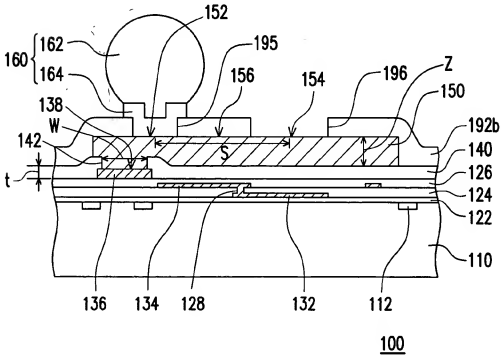


FIG. 1B

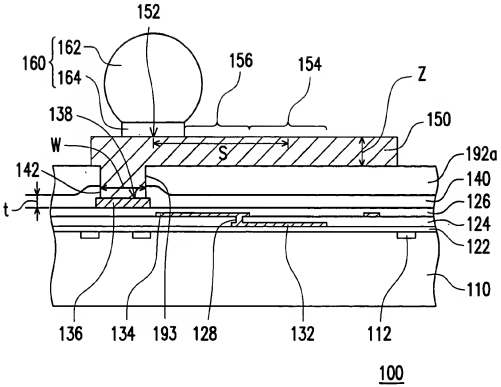


FIG. 1C

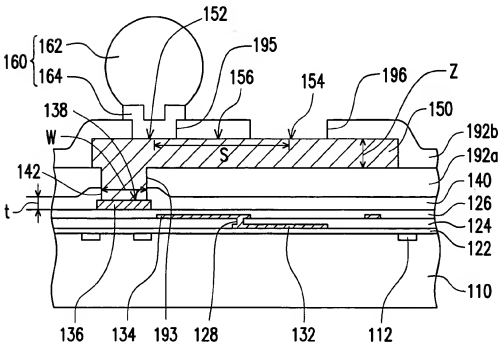


FIG. 1D

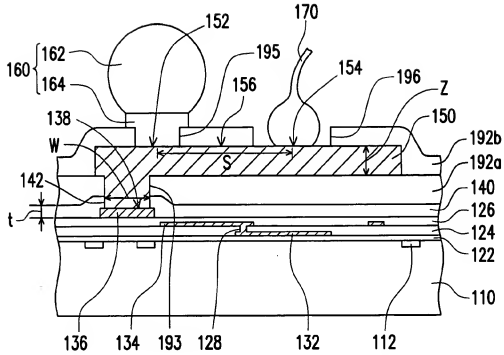
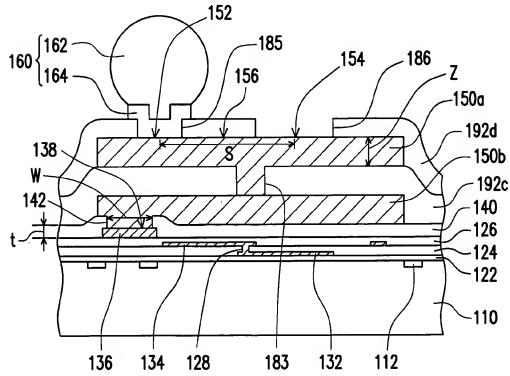


FIG. 1E 100



100

FIG. 1F

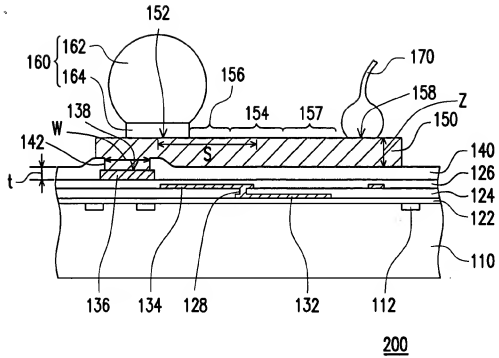


FIG. 2A

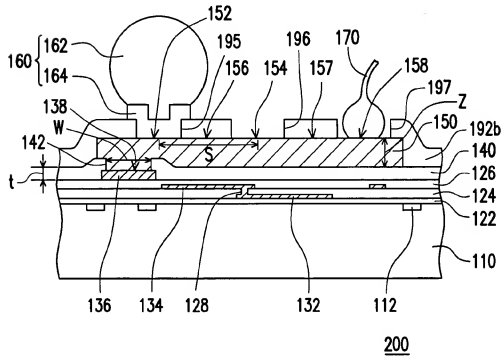


FIG. 2B

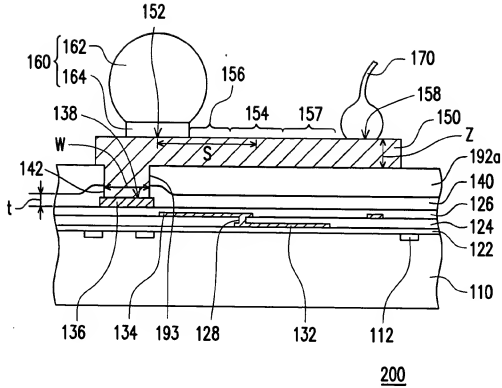


FIG. 2C

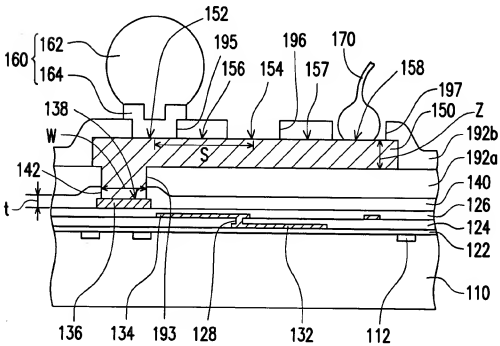


FIG. 2D

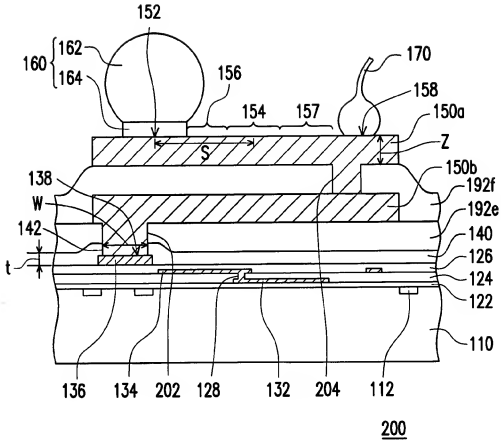


FIG. 2E

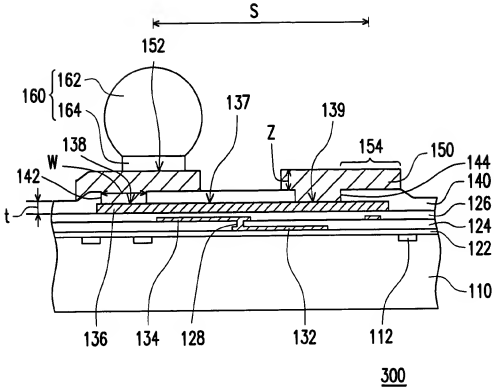


FIG. 3A

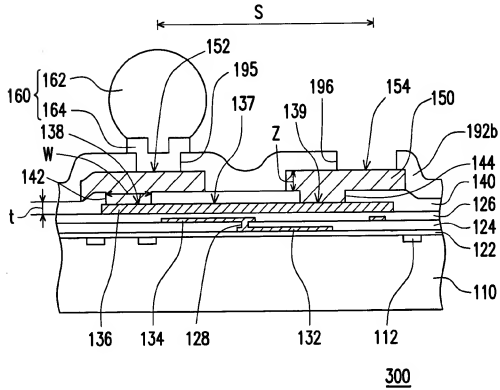


FIG. 3B

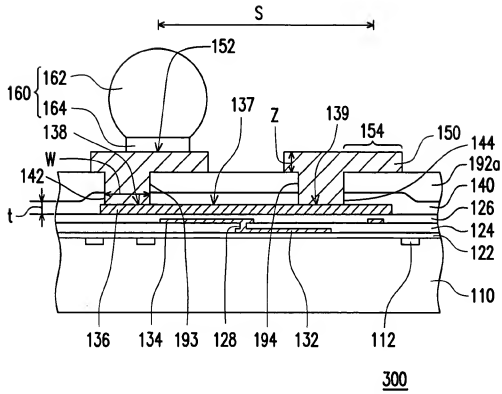


FIG. 3C

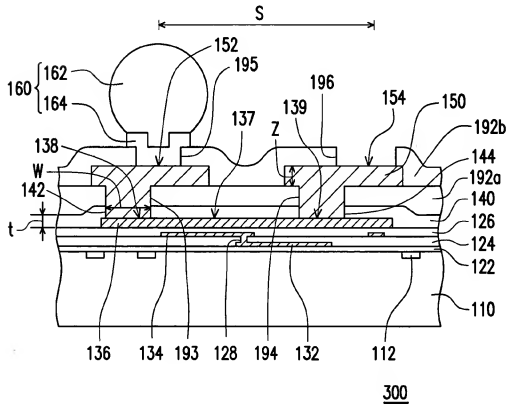


FIG. 3D

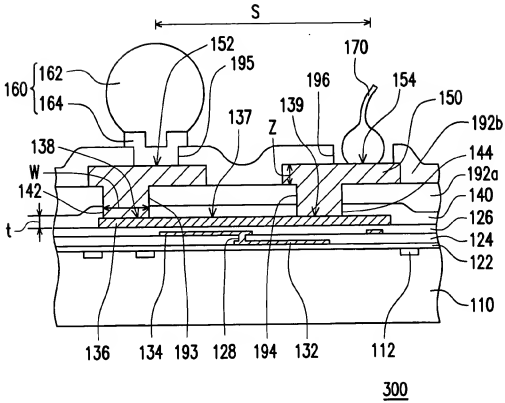


FIG. 3E

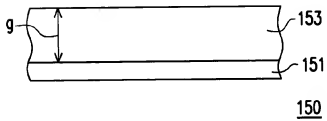


FIG. 4